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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,431	11/28/2003	Takayuki Kondo	117603	7372
25944	7590	03/31/2006		
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			EXAMINER PEACE, RHONDA S	
			ART UNIT 2874	PAPER NUMBER

DATE MAILED: 03/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No. 10/722,431	Applicant(s) KONDO, TAKAYUKI	
	Examiner Rhonda S. Peace	Art Unit 2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-6, 8, 9 and 11-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2-6, 8, 9 and 12-23 is/are rejected.
- 7) ☒ Claim(s) 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/13/2006 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8, 12, and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Pertaining to claim 8 (directly dependent upon independent claim 16), claim 8 recites, "at least part of the optical waveguide covering being at least one of the first micro-tile shaped elements and the second micro-tile shaped elements." However, claim 16 does not recite first and second micro-tile shaped elements, and instead recites first and second circuit blocks. Therefore there exists a lack of antecedent basis for the term "micro-tile shaped elements." Examination of claim 8 has proceeded, with the Examiner assuming the reference to first and second micro-tile shaped elements in claim 8 is instead referring to the first and second circuit blocks (i.e. the term "micro-tile

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shaped element" is replaced with the term "circuit block.") In addition, the wording of claim 8 suggests the current invention includes a device that serves as an "optical waveguide covering." However, from the Applicant's disclosure, the Examiner is of the opinion that claim 8 is discussing that at least a portion of the optical waveguide may cover a portion of either the first or second circuit block or both. Examination of claim 8 has proceeded under such an assumption. Appropriate correction to clarify these discrepancies is required.

Regarding claim 12 (directly dependent upon independent claim 16), claim 12 recites, "the plurality of integrated circuit chips being optically connected to each other at least through the micro-tile shaped elements." However, as previously discussed, claim 16 makes no mention of any micro-tile shaped elements. Therefore there exists a lack of antecedent basis for the term "micro-tile shaped elements." Examination of claim 12 has proceeded under the assumption that "first and second circuit blocks" should replace the term "micro-tile shaped elements". Appropriate correction to clarify this discrepancy is required.

Addressing claim 22 (dependent upon claim 20, where claim 20 is dependent upon independent claim 19), claim 22 recites "the first light emitting element and the second light emitting element being included in a second circuit block." However, claim 20 refers to the first and second light emitting elements as being disposed in a first circuit block. At this time, it is difficult to determine if the Applicant intends claim 22 to claim first and second light emitting elements to be disposed in the first circuit block, or if the Applicant intends claim 22 to recite first and second light receiving elements to be

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disposed in a second block. Reviewing the Applicant's disclosure and the wording of claim 22 as a whole, it is the opinion of the Examiner that the Applicant intends for claim 22 to recite first and second light receiving elements to be disposed in a second block. Examination of claim 22 has proceeded under such an assumption. Appropriate correction to clarify this discrepancy is required.

Claim Objections

Claims 2-6, 8, 9, and 11-15 are objected to because of the following informalities:

The above claims (all directly dependent upon the limitations of claim 16) all recite the phrase "wavelength multiplexing on-chip optical interconnection circuit." However, claim 16 simply refers to the current invention as "an optical interconnection circuit." It is the opinion of the Examiner that while this discrepancy is relatively minor, correction of claims 2-6, 8, 9, and 11-15 so that these device descriptors are in agreement will lead to a clearer presentation of the Applicant's invention. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2, 6, 12, and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimoda (US 6430325).

Pertaining to claim 16, Shimoda discloses an optical interconnection circuit comprising the following:

- An integrated circuit chip, such as a LSI circuit or a TFT circuit (column 13 lines 38-43, hereafter indicated as 13:38-43).
- A first circuit block **81(A)** provided on the integrated chip, and having a first light emitting element **301** (13:44-52, Fig 13).
- A second circuit block **82(B)** provided on the integrated chip, and having a first light receiving element **501** (13:44-52, Fig 13).
- An optical waveguide **401** on the integrated chip that optically connects the first light emitting element **301** to the first light receiving element **501** (13:53-56, Fig 13).

Addressing claims 2 and 6, Shimoda discloses the circuit blocks **81(A)** and **82(B)** are optically connected to one another, for example through waveguide **401** (13:53-56, Fig 13), and are also electrically connected to one another (see abstract, 14:14-17). Moreover, Shimoda discloses the light transmitting element **301** typically is formed using only one type of light (14:26-28), and therefore that light will have a predetermined wavelength, and the light receiving element will receive the light of this predetermined wavelength, as it has been established that light generated by element **301** is received by element **501** via waveguide **401** (13:63-65, Fig 13). Additionally, each of the circuit blocks **81(A)** and **82(B)** are each electrically connected to the integrated chip via the driving circuit **11** (for block **81(A)**) and the amplifying circuit **601** (for block **82(B)**) (13:44-52, 14:18-19, 7:43-51 and 66-67, 8:1-5, Figs 1 and 13).

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Regarding claims 14 and 15, Shimoda discloses the device described above can both convert electrical signals to optical signals (such as at light transmitter **301**, see 13:44-47) and transmit electrical signals to the integrated circuit (such as through amplifying circuit **601**, see 14:14-17, 7:66-67, 8:1-5), the device described above may be considered (in and of itself) both an electro-optical device and an electrical device, and therefore any apparatus incorporating a device as described above would also be considered both an electro-optical and an electrical apparatus.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3-5, 8, 9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoda (US 6430325).

Pertaining to claims 3-5 and 8, Shimoda discloses the device as described above. Notice that in Figure 13, Shimoda shows the waveguide 401 as being placed between the circuit blocks 81(A) and 82(B). While this is the only orientation shown for the waveguide 401, it would have been obvious to one of ordinary skill in the art to fashion the waveguide 401 in various other manners, as Shimoda explains that the waveguide 401 may also be fashioned in two and three dimensional orientations (14:62-67, 15:1-6). The important feature of the waveguide 401 is that it optically connects the first circuit block 81(A) to the second circuit block 82(B). Any manner by which this optical connection is accomplished, whether a portion the waveguide is provided on the top surfaces of the circuit blocks (so as to cover them), or a portion of the waveguide is provided on the circuit blocks so as to traverse them, or a portion of the waveguide is provided to detour the circuit blocks, is considered obvious to one of ordinary skill in the art due to the possible two and three dimensional (in addition to the one dimensional) waveguide orientations discussed by Shimoda (14:62-67, 15:1-6). In addition, modification of the waveguide from the orientation shown in Figure 13 would allow the device to be further refined to optimize optical connection between the two circuit blocks and minimize size, thereby improving overall performance and applicability of the device.

Addressing claim 9, Shimoda discloses the device as described above. However, Shimoda does not disclose the specific use of a CPU, memory circuit, DSP, RF amplifying circuit, image sensor, or bio sensor as the circuit blocks 81(A) and 82(B). However, it would have been obvious to one of ordinary skill in the art to use any of the

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above circuits as the circuit blocks **81(A)** and **82(B)**, as all are well known components which may act as circuit blocks, and in addition, further specification of the components of the device as described by Shimoda will allow the device to be applied to several differing applications

Regarding claims 12 and 13, Shimoda discloses the device as described above including that device described above may be applied to optical signal transmission between circuit blocks **81(A)** and **82(B)**, where the plurality of circuit blocks are formed on two separate semiconductor chips (14:35-45), thereby allowing the chips to be optically connected. Shimoda does not disclose *mounting these communicating semiconductor chips on a common substrate, or tightly bonding the chips to one another*. However, it would have been obvious to one of ordinary skill in the art to mount the communicating chips on a common substrate so that the optical waveguides connecting the circuit blocks of differing chips can be mounted upon the common substrate, thereby allowing for a more reliable optical connection between the circuit blocks. It would also have been obvious to one of ordinary skill in the art to bond the chips tightly to one another, as this will further decrease the size of the overall device making it more applicable to compact applications, as well as further ensuring a reliable optical connection between the chips.

Claims 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoda (US 6430325) in further view of White (US 6839481).

Pertaining to claim 17, Shimoda discloses the device as described above. In addition, Shimoda discloses the above device may further include a plurality of light

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emitting elements on the first circuit block **81(A)**, and a plurality of light receiving elements on the second circuit block **82(B)** (15:1-3). Moreover, the light emitting elements are not confined to operate at a single wavelength, as numerous lights having differing peak wavelengths may be used (14:26-34). As the first light receiver **501** (on **82(B)**) receives the first light from first light emitter **301** (on **81(A)**) along waveguide **401**, so would a second light receiver (on **82(B)**) receive a second light from a second light emitter (on **81(A)**) via a waveguide separate from waveguide **401**, where the first and second lights may be of differing wavelengths, as discussed above. However, Shimoda *does not disclose transmitting both the first and second lights along the same waveguide*. White discloses a high capacity optical multi/demultiplexing device that transmits signals of various wavelengths simultaneously and bi-directionally along a common waveguide **41** (8:50-60). It would have been obvious to one of ordinary skill in the art to transmit the signals of varying wavelength generated by the plurality of light emitters of the first circuit block to the second circuit block via a fiber as described by White, because the fiber of White allows increased capability of the device, as it operates under a broader wavelength range (4:36-43) and additionally allows for the device of Shimoda to eliminate several waveguides (as all signals can be transmitted on a single guide as opposed to a plurality of guides), thereby minimizing the cost, size, and production time associated with the device, and also allows for a more reliable optical connection between the circuit blocks, as only one waveguide must be optically coupled between the blocks as opposed to many.

Regarding claim 18, Shimoda discloses the device as described above. Further, Shimoda discloses the first circuit block **81(A)** is provided with a light receiving element **502** and the second circuit block **82(B)** is provided with a light transmitting element **302**, where elements **502** and **302** are optically connected via waveguide **402** (13:44-52, Fig 13). As previously mentioned, the light emitting elements of the device are not confined to operate at a single wavelength, as numerous lights having differing peak wavelengths may be used (14:26-34). As the first light receiver **501** (on **82(B)**) receives the first light from first light emitter **301** (on **81(A)**) along waveguide **401**, so would light receiver **502** (on **81(A)**) receive a second light from light emitter **302** (on **82(B)**) via waveguide **402** (13:61-67), where the first and second lights may be of differing wavelengths, as discussed above. However, Shimoda *does not disclose transmitting both the first and second lights along the same waveguide*. White discloses a high capacity optical multi/demultiplexing device that transmits signals of various wavelengths simultaneously and bi-directionally along a common waveguide **41** (8:50-60). It would have been obvious to one of ordinary skill in the art to transmit the signals of varying wavelength generated by the plurality of light emitters of the first circuit block to the second circuit block via a fiber as described by White, because the fiber of White allows increased capability of the device, as it operates under a broader wavelength range (4:36-43) and additionally allows for the device of Shimoda to eliminate several waveguides (as all signals can be transmitted on a single guide as opposed to a plurality of guides), thereby minimizing the cost, size, and production time associated with the device, and

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also allows for a more reliable optical connection between the circuit blocks, as only one waveguide must be optically coupled between the blocks as opposed to many.

Addressing claim 19, and summarizing the above discussion, Shimoda discloses an optical interconnection device having a plurality of light emitting elements (13:44-52, 15:1-3, Fig 13), where each emitter (one which transmits a first light, and one which transmits a second light) may operate under a different wavelength (14:26-34). The disclosure of Shimoda calls for each light to be transmitted along a single waveguide (13:53-60, 15:1-3). However, Shimoda *does not disclose transmitting both the first and second lights along the same waveguide*. White discloses a high capacity optical multi/demultiplexing device that transmits signals of various wavelengths simultaneously and bi-directionally along a common waveguide **41** (8:50-60). It would have been obvious to one of ordinary skill in the art to transmit the signals of varying wavelength generated by the plurality of light emitters via a single fiber as described by White, because the fiber of White allows increased capability of the device, as it operates under a broader wavelength range (4:36-43) and additionally allows for the device of Shimoda to eliminate several waveguides (as all signals can be transmitted on a single guide as opposed to a plurality of guides), thereby minimizing the cost, size, and production time associated with the device, and also allows for a more reliable optical connection, as only one waveguide must be optically coupled between the blocks as opposed to many.

With respect to claim 20, Shimoda in view of White discloses the device as described above. Moreover, Shimoda discloses each circuit block, such as the first

81(A), may contain a plurality of light emitters (13:44-52, 15:1-3). Figure 13 illustrates an embodiment showing only one light emitter **301** on the first circuit block **81(A)**. Emitter **301** is driven by a first driving circuit **11** (13:44-52), and therefore similar light emitters placed on the first circuit block **81(A)** would also be driven by an additional circuit similar to driving circuit **11**.

Regarding claim 22, Shimoda in view of White discloses the device as described above, including that a first emitter **301** (on first circuit block **81(A)**) will emit a first light which is then received by a first receiving element **501** on the second circuit block **82(B)** (13:53-60, Fig 13). Similarly, an additional (or second) light emitter provided on first circuit block **81(A)** would transmit a second light to an additional (or second) light receiving element provided on the second circuit block **82(B)** (13:61-67, 15:1-3). As the light receiving element **501** is driven by a (third) circuit **601** (13:44-51), any additional light receiving elements provided on the second circuit block **82(B)** would also be driven by their own circuit similar to circuit **601**. As discussed above, White discloses a waveguide that may replace the waveguides of Shimoda so that all signals may be transmitted bi-directionally along a common waveguide for the reasons discussed above.

Pertaining to claim 21, Shimoda in view of White discloses the device as described above. To summarize, the first light emitting element **301** (emitting a first light) is disposed upon the first circuit block **81(A)** and driven by a first circuit **11**, and the second light emitting element **302** (emitting a second light) is disposed upon the second circuit block **82(B)** and driven by a second circuit **12** (13:44-51, Fig 13). These signals

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may be transmitted along a common waveguide by incorporation of the teachings of White, as described above.

Addressing claim 23, Shimoda in view of White discloses the device as described above. Moreover, the first light receiving element **502** (disposed on the first circuit block **82(A)**) receives the second light emitted by second emitter **302** of the second circuit block **82(B)**, and a second light receiving element **501** (disposed on the second circuit block **82(B)**) receives the first light emitted by first emitter **301** of the first circuit block **81(A)**. As discussed above, all signals may be transmitted over a common waveguide, such as the waveguide of White, for the reasons discussed above. In addition, Shimoda discloses the first circuit block **81(A)** has a third circuit **602** to drive the first light receiving element **502**, and the second circuit block **82(B)** has a fourth circuit **601** to drive the second light receiving element **501** (13:44-51, 7:66-67, 8:1-5).

Allowable Subject Matter

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The applicable prior art does not disclose, nor does it reasonably suggest an optical interconnection circuit having a plurality of circuit blocks disposed thereon optically connected via a waveguide so that a light signal (generated by a light emitter) from one circuit block will be transmitted to the other circuit block where it will be received (by a light receiver), and *further having a plurality of micro-tiled shaped*

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elements disposed on each of the circuit blocks for the purposes of transmitting and receiving optical signals of varying wavelength.

Response to Arguments

Applicant's arguments with respect to claims 1-6, 9, and 13-15 have been considered but are moot in view of the new ground(s) of rejection set forth above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shimoda (US 2003/0026517) discloses a light transmission device provided for on an integrated chip.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rhonda S. Peace whose telephone number is (571) 272-8580. The examiner can normally be reached on M-F (8-5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on (571) 272- 2344. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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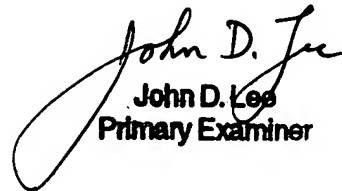
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Rhonda S. Peace

Examiner

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John D. Lee
Primary Examiner